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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,999	04/15/2004	David Dosung Chun	AMKOR-103A	7239

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EXAMINER	
THAI, LUAN C	
ART UNIT	PAPER NUMBER
2891	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,999	CHUN, DAVID DOSUNG	
	Examiner	Art Unit	
	Luan Thai	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/2/04&8/4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election *without traverse* of Embodiment II corresponding to claims 11-20, filed 10/27/06, is acknowledged.

Priority

2. This application appears to be a division of Application No. 08/813467, filed March 10, 1997.

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

4. The Information disclosure Statements filed on 8/2/04 and 8/4/04 have been considered.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 11-13 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirasawa et al. (US 2002/0020906 hereinafter "Hirasawa").

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 11-13 and 15-20, Hirasawa discloses (see specifically figures 4-5) a method of fabricating a semiconductor device, comprising the steps of: providing a lead frame (10b) having a die pad (13b), a plurality of contacts (14) defining opposed top and bottom

contact surfaces, and a plurality of conductive traces which extend from respective ones of the contacts toward the die pad (see Figs. 4A-4C); attaching at least one semiconductor die (17) to the die pad (13b) and electrically connecting the die to at least one of the conductive traces via bonding wires (19); forming a first body section (20) on the lead frame which encapsulates the semiconductor die (17) and the die pad (13b) of the lead frame other than for the contacts (14) thereof; and forming a second body section (21) on the lead frame which partially encapsulates the contacts (14) such that at least portions of the bottom contact surfaces of the contacts (14) are exposed in an exterior surface of the second body section (21), wherein the first and second body sections are formed from a common sealing resin material. Hirasawa further discloses the conductive traces being bent such that the die pad and the contacts extend along respective ones of spaced, generally parallel planes (Fig. 5E), and the step forming the second body section such that the exterior surface thereof is generally planar and the bottom contact surfaces of the contacts are exposed in and substantially flush with the exterior surface, and wherein the first body section to define a first sloped side surface, and the second body section to define a second sloped side surface which is abutted against the first sloped side surface and has an angle complimentary thereto (See Fig. 5E).

Although Hirasawa does not teach that such method steps, as described above, are using for forming a memory card, one of ordinary skilled in the art would have been obvious to apply such method in fabricating a memory card since the claimed structure in claims 11-13 and 15-20 do not distinguish over the Hirasawa reference and such application is held to be within the ordinary designing ability expected of a person skilled in the art.

7. Claims 11-13, 15-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okuaki (JP 361071652A).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 11-13, 15-18 and 20, Okuaki discloses (see specifically figure) a semiconductor device, comprising: a lead frame having a die pad (3), a plurality of contacts (32) defining opposed top and bottom contact surfaces, and a plurality of conductive traces (1) which extend from respective ones of the contacts toward the die pad (3); attaching at least one semiconductor die (4) to the die pad (3) and electrically connecting the die to at least one of the conductive traces via bonding wires (5); forming a first body section (30) on the lead frame which encapsulates the semiconductor die (4) and the die pad (3) of the lead frame other than for the contacts (32) thereof; and forming a second body section (31) on the lead frame which partially encapsulates the contacts (32) such that at least portions of the bottom contact surfaces of the contacts (32) are exposed in an exterior surface of the second body section (31), wherein the first and second body sections are formed from a common sealing resin material. Okuaki further discloses the conductive traces being bent such that the die pad (3) and the contacts (32) extend along respective ones of spaced, generally parallel planes (see Fig. 1), and the second body section having the exterior surface thereof being generally planar and the bottom contact surfaces of the contacts are exposed in and substantially flush with the exterior surface, and wherein the first body section to define a first sloped side surface, and the second body section to define a second sloped side surface which is abutted

against the first sloped side surface and has an angle complimentary thereto (See Fig. 1). It should be noted that although claims 11-13, 15-18 and 20 are "method claims", the method steps consist of the broad steps of "Providing...., connecting...., forming.....etc.", therefore these steps would be inherently satisfied by the apparatus of the reference as modified.

Although Okuaki does not teach that such device being a memory card, the structure in claims 11-13, 15-18 and 20 do not distinguish over the Okuaki reference and it has been held that a recitation (e.g., of fabricating a memory card) with respect to the manner in which a claimed method is intended to be employed does not differentiate the claimed method from a prior art method satisfying the claimed structural limitations. *Ex Parte Masham*, 2 USPQ F.2d 1647 (1987).

8. Claims 11-13 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miks et al (6,910,635) in view of Kanatake (US 2002/0020923).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 11-13 and 15-20, Miks discloses (see specifically figures 2-5) a method of fabricating a memory card, comprising the steps of: providing a lead frame (14) having a die pad (18) and tie bars (26) connected to the die pad, a plurality of contacts (20) defining opposed top and bottom contact surfaces (See Fig. 5), and a plurality of conductive traces (22) which extend from respective ones of the contacts toward the die pad (see Figs. 3); attaching at least one semiconductor die (28) to the die pad (18) and electrically connecting the die to at least one of the conductive traces via bonding wires (32); forming a first body section (34/54) on the lead

frame which encapsulates the semiconductor die (28) and the die pad (18) of the lead frame other than for the contacts (20) thereof, such that at least portions of the bottom contact surfaces of the contacts (20) are exposed in an exterior surface of the first body section (34/54). Miks further discloses the conductive traces being bent such that the die pad (18) and the contacts (20) extend along respective ones of spaced, generally parallel planes (Fig. 5), and the step forming the first body section such that the exterior surface thereof is generally planar and the bottom contact surfaces of the contacts are exposed in and substantially flush with the exterior surface, and wherein the first body section to define a first sloped side surface (See Fig. 2). Miks fails to teach forming a second body section on the lead frame, which partially encapsulates the contacts such that at least portions of the bottom contact surfaces of the contacts are exposed in an exterior surface of the second body section.

Kanatake while related to a similar method of encapsulating a semiconductor device mounted on a lead frame teaches (see specifically figures 3 and 8A) a step of forming a second body section (17) on the lead frame (12a), which partially encapsulates the contacts (12) such that at least portions of the bottom contact surfaces of the contacts are exposed in an exterior surface of the second body section and the second body section to define a second sloped side surface which is abutted against the first sloped side surface of the first body section and has an angle complimentary thereto. The purpose of forming a second body section is to prevent the semiconductor die from being contaminated by the first body section, no characteristics of the device are deteriorated and no difference in a level by the dislocation of the end of the lead terminal is caused, and a state that mounting is impossible can be prevented (paragraph [0019]).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Kanatake's process with Miks' invention would have been beneficial because the second body section, as taught by Kanatake, helps to prevent the semiconductor die from being contaminated by the first body section, no characteristics of the device are deteriorated and no difference in a level by the dislocation of the end of the lead terminal is caused, and a state that mounting is impossible can be prevented.

9. Claims 11-13 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miks et al (6,910,635) in view of Bolken (6,444,501).

Regarding claims 11-13 and 15-20, Miks discloses (see specifically figures 2-5) a method of fabricating a memory card, comprising the steps of: providing a lead frame (14) having a die pad (18) and tie bars (26) connected to the die pad, a plurality of contacts (20) defining opposed top and bottom contact surfaces (See Fig. 5), and a plurality of conductive traces (22) which extend from respective ones of the contacts toward the die pad (see Figs. 3); attaching at least one semiconductor die (28) to the die pad (18) and electrically connecting the die to at least one of the conductive traces via bonding wires (32); forming a first body section (34/54) on the lead frame which encapsulates the semiconductor die (28) and the die pad (18) of the lead frame other than for the contacts (20) thereof, such that at least portions of the bottom contact surfaces of the contacts (20) are exposed in an exterior surface of the first body section (34/54). Miks further discloses the conductive traces being bent such that the die pad (18) and the contacts (20) extend along respective ones of spaced, generally parallel planes (Fig. 5), and the step forming the first body section such that the exterior surface thereof is generally planar and the bottom contact surfaces of the contacts are exposed in and substantially flush with the exterior surface, and

wherein the first body section to define a first sloped side surface (See Fig. 2). Miks fails to teach forming a second body section on the lead frame, which partially encapsulates the contacts such that at least portions of the bottom contact surfaces of the contacts are exposed in an exterior surface of the second body section.

Bolken while related to a similar method of fabricating a memory card teaches (see specifically figures 4-4B and 8-9) an improvement to use two molding steps which includes a step of forming a second plastic body section (28) on the lead frame substrate (Col. 2, lines 40+), which partially encapsulates the contacts (24) such that at least portions of the bottom contact surfaces of the contacts are exposed in an exterior surface of the second plastic body section and the second plastic body section to define a second sloped side surface which is abutted against the first sloped side surface of the first plastic body section (26) and has an angle complimentary thereto (See Figs. 4A-4B). The purpose of applying two molding steps is to eliminate the need for glop top, cap molding and cap attachment, to make available a variety of options not otherwise available, to effectively eliminate resin bleed into areas intended to be left uncovered, and to enhance a degree of dimensional uniformity and reliability (Col. 2, lines 23-34).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Bolken's process with Miks' invention would have been beneficial because the two molding steps method, as taught by Bolken, helps to eliminate the need for glop top, cap molding and cap attachment, to make available a variety of options not otherwise available, to effectively eliminate resin bleed into areas intended to be left uncovered, and to enhance a degree of dimensional uniformity and reliability.

10. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miks et al (6,910,635) and Kanatake (US 2002/0020923), as applied to claims 11-13, and further in view of either Kawai et al (US 2003/0127711) or Glenn et al (6,455,356).

Regarding claim 14, the proposed method of Miks and Kanatake discloses the claimed invention as detailed above except for the conductive traces being etched to have a thickness, which is less than a contact thickness and the die pad thickness.

Kawai while related to a method of molding a chip on lead frame discloses (See Figs. 10A-10C and 11A-11C) that the conductive traces (103) being etched to have a thickness, which is less than a contact thickness of the contacts (104) and the die pad thickness of the die pad (106). Similarly, Glenn while related to a method of molding a chip on lead frame discloses (See Figs. 3-6) that the conductive traces (33) being etched to have a thickness, which is less than a contact thickness of the contacts (32) and the die pad thickness of the die pad (22). The purpose of doing so would have helped to prevent the die pad and the conductive traces from being pulled vertically from the package body (See Glenn's Abstract, lines 11+).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining either Kawai's process or Glenn's process with the proposed method of Miks and Kanatake would have been beneficial because it helps to prevent the die pad and the conductive traces from being pulled vertically from the package body.

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miks et al (6,910,635) and Bolken (6,444,501), as applied to claims 11-13, and further in view of either Kawai et al (US 2003/0127711) or Glenn et al (6,455,356).

Regarding claim 14, the proposed method of Miks and Bolken discloses the claimed invention as detailed above except for the conductive traces being etched to have a thickness, which is less than a contact thickness and the die pad thickness.

Kawai while related to a method of molding a chip on lead frame discloses (See Figs. 10A-10C and 11A-11C) that the conductive traces (103) being etched to have a thickness, which is less than a contact thickness of the contacts (104) and the die pad thickness of the die pad (106). Similarly, Glenn while related to a method of molding a chip on lead frame discloses (See Figs. 3-6) that the conductive traces (33) being etched to have a thickness, which is less than a contact thickness of the contacts (32) and the die pad thickness of the die pad (22). The purpose of doing so would have helped to prevent the die pad and the conductive traces from being pulled vertically from the package body (See Glenn's Abstract, lines 11+).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining either Kawai's process or Glenn's process with the proposed method of Miks and Bolken would have been beneficial because it helps to prevent the die pad and the conductive traces from being pulled vertically from the package body.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 8:00 AM - 4:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Luan Thai/

Luan Thai
Primary Examiner
Art Unit 2891
January 9, 2007